

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 18

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ATSUSHI KAWASAKI, KOHEI EGUCHI,
KATSUKI HAZAMA, and FUMITAKA SUGAYA

Appeal No. 1998-3043
Application 08/667,587¹

ON BRIEF

Before McKELVEY, Senior Administrative Patent Judge, and
LEE and MEDLEY, Administrative Patent Judges.

LEE, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's rejection of appellants' claims 7-10, 12-17, and 25-35. Claims 18-24 have been withdrawn from consideration and claims 1-6 and 11 have been canceled. No claim has been allowed.

References relied on by the Examiner

Tanaka et al. (Tanaka) U.S. Patent 5,290,725 March 1, 1994

¹ Application for patent filed June 24, 1996. The real party in interest is Nippon Steel Corporation.

Appeal No. 1998-3043
Application 08/667,587

Chen et al. (Chen) U.S. Patent 4,905,073 Feb. 27, 1990

The Rejection on Appeal

Claims 7-10, 12-17, and 25-35 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Tanaka and Chen.

The Invention

The claimed invention is directed to a semiconductor device. Independent claims 25, 29, and 10 are reproduced below:

25. A semiconductor device comprising a semiconductor substrate, first and second wells of first and second conductivity types formed so as to be adjacent to each other in a surface portion of said substrate, and a plurality of MOS transistors formed in at least one of said wells, each of said transistors having source/drain regions of a conductivity type opposite to that of said one well, wherein:

said MOS transistors are electrically isolated from one another by a field-shield isolation structure; and

said first and second wells are electrically isolated from each other by a first field oxide film.

29. A semiconductor device comprising a semiconductor substrate and a plurality of wells formed in a surface portion of said substrate, wherein:

each of said wells is electrically isolated from a different one of the wells and from said semiconductor substrate by a field oxide film, and elements formed in said wells are electrically

isolated from one another by a field-shield isolation structure.

10. A semiconductor device comprising:

a semiconductor substrate having a main surface;

first, second and third field oxide films formed in said main surface of said semiconductor substrate, each of said field oxide films having an inner surface located within said semiconductor substrate;

first and second semiconductor regions defined in said semiconductor substrate, said first and second semiconductor regions having first and second conductivity types, respectively, and being arranged to form a first junction therebetween, said first junction terminating at said inner surface of said first field oxide film, whereby said first and second semiconductor regions are isolated from each other;

a third semiconductor region having the second conductivity type and being defined in said semiconductor substrate to be spaced from said second semiconductor region, said second and third semiconductor regions forming second and third junctions with said semiconductor substrate, respectively, said second and third junctions terminating at said inner surface of said second field oxide film, whereby said second and third semiconductor regions are isolated from each other;

a fourth semiconductor region having the first conductivity type and being defined in said third semiconductor region to form a fourth junction therewith, said fourth junction terminating at said inner surface of said third field oxide film, whereby said fourth semiconductor region is isolated from said third semiconductor region; and

a first connection conductor formed over said main surface of said semiconductor substrate for electrically connecting a first circuit element in said first semiconductor region and a second circuit element in said second semiconductor region, said first connection conductor being in contact with and extending on said first field oxide film to cross over said first junction between said first and second semiconductor regions, and a second connection conductor formed over said main surface of said semiconductor substrate for electrically connecting a third circuit element in said third semiconductor region and a fourth circuit element in said fourth semiconductor region, said second connection conductor being in contact with and extending on said third field oxide film to cross over said fourth junction between said third and fourth semiconductor regions.

Opinion

The rejection of claims 7-10, 12-17, and 25-35 is reversed.

A reversal of the rejection on appeal should not be construed as an affirmative indication that the appellant's claims are patentable over prior art. We address only the positions and rationale as set forth by the examiner and on which the examiner's rejection of the claims on appeal is based.

According to the appellants (Br. at 6), all of the claims on appeal require that semiconductor regions formed in the semiconductor substrate are isolated from each other and from the substrate by a field oxide film, while circuit elements

Appeal No. 1998-3043
Application 08/667,587

formed within each region are isolated from each other by "field shield structures." That assertion is incorrect with respect to independent claim 10 and claims 12 and 34 which depend from claim 10. Accordingly, we will address claims 10, 12, and 34 separately from all other claims.

With regard to all claims on appeal except for claims 10, 12, and 34, the determinative issue centers about the meaning of

the claim term "field-shield isolation structure." We look first to the appellants' specification.

In the section of the specification entitled Background of the Invention, the appellants discuss methods for isolating circuit elements in a semiconductor device. From page 1, line 16 to page 2, line 14, it is stated:

A so-called "field-shield isolation" method, which isolates elements by a MOS structure formed on a semiconductor substrate, has been proposed as an isolation method which does not generate the bird's beaks.

Generally, the field-shield isolation structure has a MOS structure in which shield gate electrodes made of a polycrystalline silicon (polysilicon) film are formed over a silicon substrate through a shield gate oxide film. This shield gate electrode is always kept at a constant potential of 0 V, for example, as it is grounded (GND) through a connection conductor when the silicon substrate (or a well region) has a P type conductivity. When the silicon substrate (or the well region) has an N type conductivity, the shield gate electrode is always kept at a predetermined potential (a powerful source potential V_{cc} [V], for example).

As a result, because the formation of a channel of a parasitic MOS transistor on the surface of the silicon substrate immediately below the shield gate electrode can be prevented, adjacent elements such as transistors can be electrically isolated from one another.

We then look to extrinsic evidence submitted by the appellants in the form of an article entitled "FULLY PLANARIZED 0.5Fm

Appeal No. 1998-3043
Application 08/667,587

TECHNOLOGIES FOR 16M DRAM" in the publication IEDM and published in 1988. The discussion of "field-shield isolation" in that article on page 247 appears below and is not inconsistent with the appellants' definition of field shield isolation:

The field-shield isolation is a three layer structure consisting of a thin thermal oxide (field-shield gate oxide), a doped polysilicon (field-shield plate) deposited on the thin gate oxide and a CVD oxide layer deposited on the polysilicon plate.

In the Abstract, the article explains that field-shield isolation "enables the isolation region to reduce down to a half-micron."

In light of the foregoing, it is evident that "field-shield isolation structure" refers to the internal configurations of a semiconductor device. Of course, this structure is defined in part by what it does, but it is well established that product claims may include process steps to wholly or partially define the claimed product. See, e.g., In re Luck, 476 F.2d 650, 653, 177 USPQ 523, 525 (CCPA 1973). To the extent these process limitations distinguish the product over the prior art, they must be given the same consideration as traditional product characteristics. Id. Consider also the

Appeal No. 1998-3043
Application 08/667,587

structural elements clock, container, and switch, all of which are defined at least in part by what they do.

It is inappropriate for the examiner to disregard the claimed isolation function of the appellants' structural element "field-shield isolation structure." The cases cited by the

examiner, i.e., In re Pearson, 494 F.2d 1399, 181 USPQ 641 (CCPA 1974) and Ex parte Minks, 169 USPQ 120 (Bd. App. 1971), are not apposite, since the functions at issue there pertain only to the general field of intended use of the invention and do not help to define the structure of the claimed apparatus or compound.

The examiner cites (answer at 3) to Tanaka's floating gate electrode [4] and control gate electrode 9 as the appellants' claimed field-shield isolation structure, but makes no attempt to explain how these two elements serve to provide field-shield isolation of separate circuit elements within a common region on the semiconductor substrate. Evidently, as is pointed out by the appellants, these electrodes are not a part of any isolation structure but are themselves a part of the circuit elements a field-shield isolation structure is supposed to isolate. The fact that a field-shield isolation structure may include an electrode over an oxide film does not make any electrode over an oxide film a field-shield isolation structure. The examiner has nowhere accounted for the isolation property of the field-shield isolation structure and thus improperly ignored a very

important feature of the appellants' claimed invention.

Additionally, it should be noted that according to the appellants' specification, the gate electrode of the appellants' field-shield isolation structure must be kept at a constant potential, either at ground or at the level of the power source, depending on the type of circuit element being isolated, in order to achieve isolation. The examiner has not demonstrated that Tanaka's floating gate electrode 4 and control gate electrode 9 are confined to a fixed or constant potential.

The examiner states (answer at 5): "[I]t is not understood based upon a prior art IEDM reference how Applicant can claim novelty on this [field-shield isolation] feature. It is not understood why Applicant would cite this reference for definition purposes and then allege patentability [based] on this very feature." The short answer to that question, as indicated by the appellants (Reply from page 4, line 20 to page 5, line 1), is:

[A]pplicant does not allege patentability simply on a field shield isolation structure. All of the independent claims [except for claim 10] on appeal recite both a field oxide film and field shield isolation structures formed on the same semiconductor substrate in order to obtain a high

Appeal No. 1998-3043
Application 08/667,587

integration density and a reduction of the chip
occupation area. (Emphasis in original.)

For all of the foregoing reasons, the examiner has not
made out a prima facie case of obviousness with respect to the
appellants' claims 7-9, 13-17, 25-33 and 35. The rejection of
claims 7-9, 13-17, 25-33 and 35 cannot be sustained.

Independent claim 10 and dependent claims 12 and 34, to the extent argued by the appellants,² require the presence of a connection conductor to connect an element located in a first region on a semiconductor substrate and an element located in a second region on the semiconductor substrate where the two regions are isolated by a field oxide film and where the conductor contacts and is directly on the field oxide film. The examiner acknowledges that Tanaka fails to show interconnection across the field oxide film (answer at 4, lines 2-4), but states (answer at 4, lines 4-5): "Chen provides for such structure in the interconnection [119] between adjacent CMOS devices." The position taken by the examiner does not adequately support a conclusion of obviousness for the appellants' claimed invention. In Chen, the connection conductor 119 does not contact the field oxide film as is required by appellants' independent claim 10. (See Chen Figure 1). The examiner has made no explanation as to why it would have been obvious to one with ordinary skill in the art to incorporate a connection conductor which contacts and extends on the field oxide film. Accordingly, the

² Brief at 3, lines 17-27 and at 6, lines 23-26.

Appeal No. 1998-3043
Application 08/667,587

examiner has not set forth a prima facie case of obviousness with respect to claims 10, 12 and 34. The rejection of claims 10, 12 and 34 cannot be sustained.

Conclusion

The rejection of claims 7-10, 12-17, and 25-35 under 35 U.S.C. § 103 as being unpatentable over Tanaka and Chen is reversed.

REVERSED

FRED E. McKELVEY, Senior)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
JAMESON LEE)	APPEALS AND
Administrative Patent Judge)	INTERFERENCES
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Appeal No. 1998-3043
Application 08/667,587

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